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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,836	04/12/2004	Sandeep Pant	20-336	1754

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EXAMINER

WILLOUGHBY, TERRENCE RONIQUE

ART UNIT	PAPER NUMBER
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2836

MAIL DATE	DELIVERY MODE
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08/07/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/821,836

Applicant(s)

PANT ET AL.

Examiner

Terrence R. Willoughby

Art Unit

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-11,13-16,18-20 and 22-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-11,13-16,18-20 and 22-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 4/12/04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Applicant's amendment filed on 5/17/2007 has been entered. Accordingly Claims 2, 12, 17 and 21 have been cancelled. Claims 1, 3, 9, 13, 15, 18, 19, 22 and 23 have been amended. Claims 1, 3-11, 13-16, 18-20 and 22-35 remain pending in the application.

Specification

The disclosure objection is withdrawn based on the applicant's remarks/comments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3-7, 9-11, 13-16, 19-20, 22-24 and 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US 5,946,177) and in view of Li (US 6,639,771).

Regarding claims 1,9,15,19 and 23 Miller et al. in (Fig. 7) discloses an integrated circuit including electrical over stress shunt (col. 1, ll. 5-13) comprising:

a voltage threshold detector (325) to detect an electrical over stress event wherein a potential is measured between a higher potential power rail (305) and a lower potential ground rail (310) in excess of a predetermined voltage (col. 9, ll. 43-47); and

a switchable low resistance path (345) between said power rail (305) and said ground rail (310), said low resistance path being adapted to be switched ON for a duration of said electrical over stress event (col. 10, ll. 36-54).

Miller et al. does not explicitly disclose said electrical over stress event occurring during a difference in an order in which connections are made between contacts of a powered device and contacts of an unpowered device as they are connected or disconnected.

Li discloses an Internet ESD-shunt diode protected by delayed external mosfet switch (abstract) wherein the electrical over stress event occurs during a difference in an order in which connections are made between contacts of a powered device and contacts of an unpowered device as they are connected or disconnected (col. 1, ll. 18-20 and col. 2, ll. 12-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the integrated circuit of Miller et al. by providing some adjustment necessarily for using the circuit of Miller et al. in an environment disclosed by Lee because it would expand the market and manufacturing of Miller et al. integrated circuit device.

Miller et al. in view of Li does not disclose said low resistance path being adapted to be switched ON for a duration of said electrical over stress event lasting significantly longer than 2 microseconds.

However, Miller et al. in (Fig. 7) discloses an RC time delay circuit (340) which is the period of time determined by the RC time constant in which the low resistance shunt switch (345) will remain conductive. As a result, it is critical that this RC time constant is long enough to exceed the maximum expected duration (i.e. emphasis added) of an ESD event. The RC time constant is a result effective variable, (i.e. variable which achieves a recognized result).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set an appropriate delay time, particularly 2 or more microseconds, because as a court decision in *In Re Aller*, 220 F. 2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) states "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation".

Regarding claims 3, 4, 13, 18, 22 and 24 Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claims 1,9,15,19, and 23, wherein:

said low resistance path (Miller et al., Fig. 7, 345) is adapted to be switched ON for a duration of an electrical over stress event (col. 10, ll. 35-54), except for said low resistance path is adapted to be switched ON for longer than 1000 or 4000 microseconds.

However, Miller et al. in (Fig. 7) discloses an RC time delay circuit (340) which is the period of time determined by the RC time constant in which the low resistance shunt switch (345) will remain conductive. As a result, it is critical that this RC time constant is long enough to exceed the maximum expected duration (i.e. emphasis added) of an ESD event. The RC time constant is a result effective variable, (i.e. variable which achieves a recognized result).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set an appropriate delay time, particularly 1000 or 4000 microseconds, because as a court decision in *In Re Aller*, 220 F. 2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) states "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation".

Regarding claim 5, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claim 1, further comprising:

a driver (Miller et al., Fig. 4, 179,180) between said voltage threshold detector (Miller et al, Fig. 4, 182,183 and col. 9, ll. 22-24) and said switchable low resistance path (Miller et al., Fig. 4, 195).

Regarding claim 6, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claim 5, wherein:

said driver comprises a series connection of a plurality of inverters (Miller et al, Fig. 4, 179,180 and col. 6, ll. 51-54).

Regarding claims 7 and 14, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claims 1 and 9, wherein said switchable low resistance path comprises:

a MOSFET transistor (Miller et al., Fig. 7, 345).

Regarding claim 10, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claim 9, wherein: said integrated circuit is based on 3.3v technology (Miller et al., col. 11, 13-15).

Regarding claims 11, 16 and 20, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claims 9 and 15 and 19, wherein:

said predetermined threshold (Miller et al., col. 9, ll. 43-52) is at least 5.5 volts (Miller et al., col. 11, 13-15).

Regarding claims 31-35, Miller et al. in view of Li and in view of Whitney discloses the integrated circuit including an electrical over stress shunt according to claims 1, 9, 15, 19 and 23, wherein:

one of said powered device and said unpowered device is a connector (Li, Fig. 2, 90 and col. 2, ll. 50-67).

Claims 8 and 25-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US 5,946,177) in view of Li (US 6,639,771) as applied to claims 1 and 23 above, and further in view of Whitney et al. (US 2002/0024791).

Regarding claims 8 and 25, Miller et al. in view of Li discloses the integrated circuit including an electrical over stress shunt according to claims 1 and 23, wherein: said integrated circuit includes a interfaces for telecom and datacom applications (Li, col. 1, ll. 18-20 and col. 2, ll. 12-16).

Miller et al. and Li do not explicitly disclose a Firewire IEEE 1394 interface.

Whitney et al. discloses an electrostatic shunt circuit (abstract and para. [0002]) to protect an integrated circuit including a Firewire IEEE 1394 interface (Figs. 13A,B and page 6, para. [0093], ll. 1-4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the integrated circuit of Miller et al. and Li with the Firewire interface of Whitney et al. to protect input/output signals and to improve accessibility of the connections to the transmission lines and other lines of data transfer interfaces.

Regarding claims 26-30, Miller et al. in view of Li and in view of Whitney discloses the integrated circuit including an electrical over stress shunt according to claims 1,9,15,19 and 23, wherein:

one of said powered device and said unpowered device is a cable (Whitney et al. page 2, para, [0030 and 0045 and 0092 and 0093].

Regarding claims 31-35, Miller et al. in view of Li and in view of Whitney discloses the integrated circuit including an electrical over stress shunt according to claims 1,9,15,19 and 23, wherein:

one of said powered device and said unpowered device is a connector (Li, col. 2, ll. 59-67).

Response to Arguments

Applicant's arguments filed on 5/17/2007 have been fully considered but they are not persuasive.

In response to Applicant's argument that Miller et al. electrical circuit device (Fig. 7) is not directed to providing electrical over stress protection. However, the Examiner does not agree with this assessment. The Examiner will like to point out to the Applicant's that Miller et al. invention generally relates to providing protection against both electrostatic discharge (ESD) and electrical overstress (EOS) events (col. 1, ll. 5-7).

In response to Applicant's arguments toward the RC time delay constant (Fig. 7, 340) disclosed by Miller et al. not being long enough to protect against an EOS event lasting significantly longer than 2-3 microseconds. However, the Examiner does not agree with this assessment because Miller et al. in (Fig. 7) discloses an RC time delay circuit (340) which is the period of time determined by the RC time constant in which the low resistance shunt switch (345) will remain conductive during an over-voltage occurring between the power and ground rail. As a result, it is critical that this RC time constant is long enough to exceed the maximum expected duration of an ESD event. Further, Miller et al. discloses the RC time constant being typically a few hundred

nanoseconds. However, Miller et al. discloses it is critical that this RC time constant be long enough to exceed the maximum expected duration (i.e. emphasis added). Therefore, the RC time constant is a result effective variable, (i.e. variable which achieves a recognized result).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set an appropriate delay time, particularly 1000 or 4000 microseconds, because as a court decision in *In Re Aller*, 220 F. 2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) states "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation".

In response to Applicant's arguments toward Li not disclosing an ESD event lasting longer than 2-3 microseconds. The Examiner will like to point out that Li was not relied upon for those teachings. Li was relied upon for discloses an electrical over stress event occurring during a difference in an order in which connections are made between contacts of a powered device and contacts of an unpowered device as they are connected or disconnected (i.e. hot-swapping interfaces and col. 1, ll. 18-20 and col. 2, ll. 50-67).

In response to Applicant's arguments toward Li not disclosing an EOS event caused by other procedures, such as inserting Firewire cable. The Examiner will like to point out that Li was not relied upon for those teachings. Whitney et al. was relied upon for those teachings (para. [0002 and 0011]) (Figs. 13A,B and page 6, para. [0093], ll. 1-4).


In response to Applicant's arguments toward Whitney et al. not disclosing any type of switchable path between a power rail and ground rail. The Examiner will like to point out that Whitney was not relied upon for those teachings. Miller et al. in (Fig. 7) discloses a switchable path (345) between a power rail (305) and a ground rail (310).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terrence R. Willoughby whose telephone number is 571-272-2725. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2800 ext 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


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